Main Injector S&H Support

Sample-and-hold system logic

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This note describes Sample-and-hold support for Main Injector HLRF is supported. A number of A/D channels must be available as channels whose reading is updated only once per MI cycle—perhaps every 2–3 seconds. In addition, those same signals should also be available for Fast Time Plots using the 1 KHz digitizer support that is part of an IRM. This kind of support was already provided for Booster HLRF, so first let us review how it was handled there.

Booster S&H Logic

There are 9 analog channels that are sample-and-held on Booster beam cycles. Each such channel is also digitized at 1 KHz in the usual way of all A/D channels of an IRM. The S&H outputs are connected to different channels. To be specific, channels 0120–0128 are used for the S&H outputs. The corresponding channels that connect to the raw waveform signals are 0114–0119, 010E–0110. Each cycle, all A/D channels are first copied out of the hardware circular buffer into the data pool and assigned channels 0100–013F. Then the readings of the S&H channels are copied over the readings of the corresponding waveform signals. This means that the data pool values for the waveform channels are always a copy of the S&H channels.

Then the capture logic is performed on all channels selected to have it done, according to the capture flag bit in the analog descriptor. Capture logic senses a status bit to decide which of two actions to perform. If the status bit is set, the reading field is copied into the capture field of the data pool for that channel. If the status bit is zero, the captured reading is copied into the reading field. The status bit that is used reflects the occurrence of clock event 10, which includes any Booster Reset event. All nine signals have the capture logic enabled for both the S&H and waveform channels.

The result of the above machinations are that the data pool readings of the 9 signals, both the S&H channels and the waveform channels, have values that are updated only on Booster reset cycles. Any of these channels will reflect the S&H values on a Parameter Page display. But the waveform channels may also be used via FTPMAN to plot from the 1 KHz hardware circular buffer, allowing the waveforms of these channels to be plotted at any rate up to 1 KHz.

Main Injector S&H Logic

For Main Injector HLRF, there is a need for a sample-and-hold signal that operates once each Main Injector cycle. It will be used to trigger the sample-and-holds to latch the set of channels that are to be measured at one time during the RF cycle. In addition to triggering the hardware, following a delay after a Tevatron clock event, the software needs to know that this has occurred, so it can latch the readings into the data pool, and also be aware of the time new data is available in the data pool. The IRMs operate at 15 Hz in synchronism with the accelerator clock, but the Main Injector RF cycle is run only every few seconds. One selected time within that cycle is used for capturing the sample-and-held data that will be shown on parameter page displays. In addition, two key closed loops, MRF0 and DAC1, must know when to sample the data pool and make their adjustments once each RF cycle.

The software needs a pseudo status bit that is set on one 15 Hz cycle during a Main Injector cycle. Since the S&H delay time can be set arbitrarily, the actual time for triggering the S&H unit is of unknown phase relative to the 15 Hz cycle operation of the IRMs. The 15 Hz cycle that occurs soonest after the during which the S&H trigger occurs is suitable for sampling the S&H data for the current RF cycle.

The selection of triggering clock events and delay times are done via an IP177 Timer board. This board provides support for up to two interrupts that are triggered by the delay times for timer #0 and #1. Other timers (#2–#7) cannot generate interrupts. Timer #0 is chosen for providing the S&H trigger signal. That timer will be triggered by any of the 8 Main Injector Reset clock events (20,21,23,29,2A,2B,2D,2E). After a chosen delay time, the S&H pulse will result. The interrupt available from Timer #0 is enabled, and the interrupt code increments a counter. When task-level code detects a change in the value of this counter, a pseudo status bit is set, else it is cleared.

In the Data Access Table, an entry follows the invocation of Local Applications. This entry detects a change in the counter value and sets a pseudo status bit accordingly; if the counter changed, the status bit is set, else it is cleared.

On the next 15 Hz cycle, the A/D data is copied into the data pool as usual. The reading fields of the S&H signals are copied over the newly-refreshed readings of the waveform channels. Capture logic is performed on all selected channels, which include both the waveform channels as well as the S&H channels. After any further data Access Table processing, the Local Applications are run, including MRF0. When MRF0 detects that the pseudo status bit is set, it knows that there is fresh data available in the data pool. Note that this occurs from 1–2 cycles (15 Hz cycles) after the S&H trigger time, insuring that the data copied from the most recent set of the 1 KHz data buffer was measured after the S&H trigger.

In summary, these are the key actions that take place during Data Access Table processing:

Update digital status data pool
Access A/D data from most recent 1 KHz data set
Copy S&H channels to waveform channels
Perform capture logic for selected channels
    If pseudo status bit set, copy readings to capture field
    If pseudo status bit clear, copy capture field to reading field
Invoke all enabled local applications
Set bit if change in interrupt counter, else clear bit.